

Technical Note

DDR3 Power-Up, Initialization, and Reset

Introduction

DDR3's extensive feature set requires changes to the power-up and initialization routine for DDR3 SDRAM devices. Each time the memory is powered up, the device specifies a routine to initialize the internal state machines and to configure the numerous user-defined operating parameters. Although the routines for DDR3 are similar to those that are required in previous generations of DRAM, some differences do exist. The purpose of this technical note is to describe the differences in the power-up and initialization routines used by DDR3, to discuss the selectable modes that require special attention during initialization, and to introduce the RESET# pin and describe how to properly use it.

DDR3 Initialization Routine

The following sequence of steps is required to power up and initialize the DDR3 SDRAM device. Following these steps will ensure that the part is in a known state prior to normal operation.

Apply Power

When power is ramped, the RESET# pin should be less than $0.2 \times V_{ddq}$. Holding the RESET# pin LOW ensures that the outputs remain disabled (High-Z) and that ODT is off (Rtt is High-Z). Ensuring that Rtt is High-Z in DDR3 is one major difference between the DDR2 and DDR3 initialization routines. DDR2 requires that the ODT pin is held LOW after Vref is at a valid level, but DDR3 internally takes care of this when the RESET# pin is held LOW. RESET# is the only pin on the DDR3 device that operates with LVCMOS input levels. This enables it to internally be driven LOW independent of the voltage level of Vref. All other inputs may be undefined during this period.

During power-up, either condition A or condition B (described in the following paragraphs) must be met.

Power-Up Condition A – Single Power Source

- Vdd and Vddq are driven from a single power converter output and are ramped with a maximum delta voltage of 300mV. Slope reversal of any power supply signal is allowed. Although JEDEC supports slope reversal of the power supply in this specific condition, Micron recommends avoiding slope reversal if possible.
- To prevent latchup, the voltage levels on all balls except Vdd, Vddq, Vss, and Vssq must be less than or equal to Vddq and Vdd on one side and must be greater than or equal to Vssq and Vss on the other side. Both Vdd and Vddq power supplies must ramp to Vdd (MIN) and Vddq (MIN) within 200ms (t_{Vddpr} specification).
- Both VrefDQ and VrefCA track $Vdd \times 0.5$. Note that VrefDQ and VrefCA are isolated within the DDR3 device and do not require separate external supplies.

- Vtt is limited to 0.95V when the power ramp is complete and is not applied directly to the device. The Vtt supply should be ramped after or at the same time as Vdd to ensure that latchup does not occur.

Power-Up Condition B – Multiple Power Sources

- Vdd may be applied before or at the same time as Vddq.
- Vddq may be applied before or at the same time as Vtt, VrefDQ, and VrefCA.
- No slope reversals are allowed in the power supply ramp for this condition.

Control CKE and RESET# and Apply Stable Clock

- Until the power supplies are stable, maintain RESET# LOW to ensure the outputs remain disabled (High-Z). After the power is stable, RESET# must be LOW for at least 200 μ s to begin the initialization process. ODT will remain in the High-Z state while RESET# is LOW and until CKE is registered HIGH.
- CKE must be LOW 10ns prior to RESET# transitioning HIGH.
- After RESET# transitions HIGH, wait 500 μ s with CKE LOW.
- After the CKE LOW time, CKE may be brought synchronously HIGH while only NOP or DES commands are issued. The clock must be present and valid for at least 10ns (and a minimum of 5 clocks) and ODT must be driven LOW or HIGH at least t_{IS} prior to CKE being registered HIGH. To conserve power, Micron recommends holding ODT LOW until normal operation commences. After CKE is registered HIGH, it must be continuously registered HIGH until the full initialization process is complete.

Issue MRS Commands

After CKE is registered HIGH and t_{XPR} has been satisfied, MRS commands may be issued.

- Issue an MRS (LOAD MODE) command to MR2 with the applicable settings (provide LOW to BA2 and BA0 and HIGH to BA1).
- Issue an MRS command to MR3 with the applicable settings.
- Issue an MRS command to MR1 with the applicable settings, including enabling the DLL and configuring the ODT.
- Issue an MRS command to MR0 with the applicable settings, including a DLL RESET command. To lock the DLL, input 512 clock cycles (t_{DLLK}). While the DLL is locking, it is important to keep clock jitter to a minimum. See the DDR3 data sheet for the period and cycle-to-cycle jitter specifications that are required to effectively lock the DLL.

Calibrate Rtt and Ron

Issue a ZQCL command to calibrate Rtt and Ron values for PVT. Prior to normal operation, t_{ZQinit} must be satisfied. When t_{DLLK} and t_{ZQinit} have been satisfied, the DDR3 SDRAM is ready for normal operation.

Figure 1: Initialization Routine

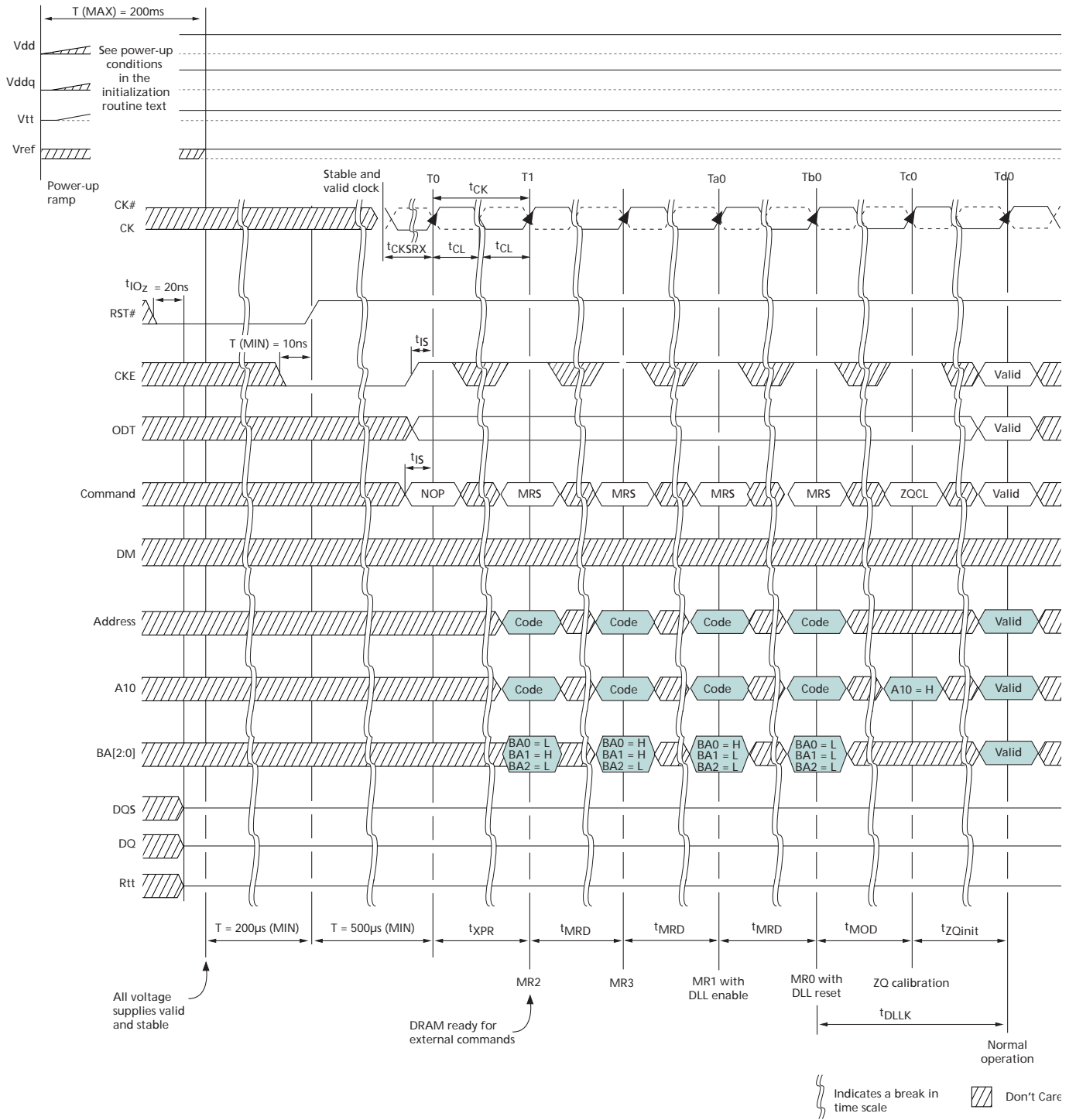
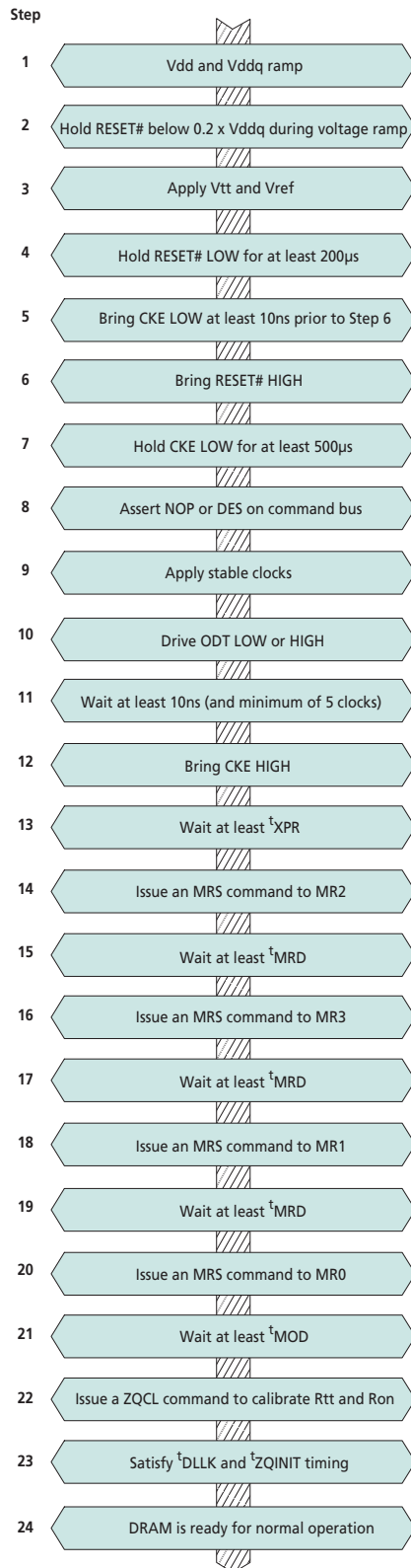


Figure 2: Initialization Flowchart



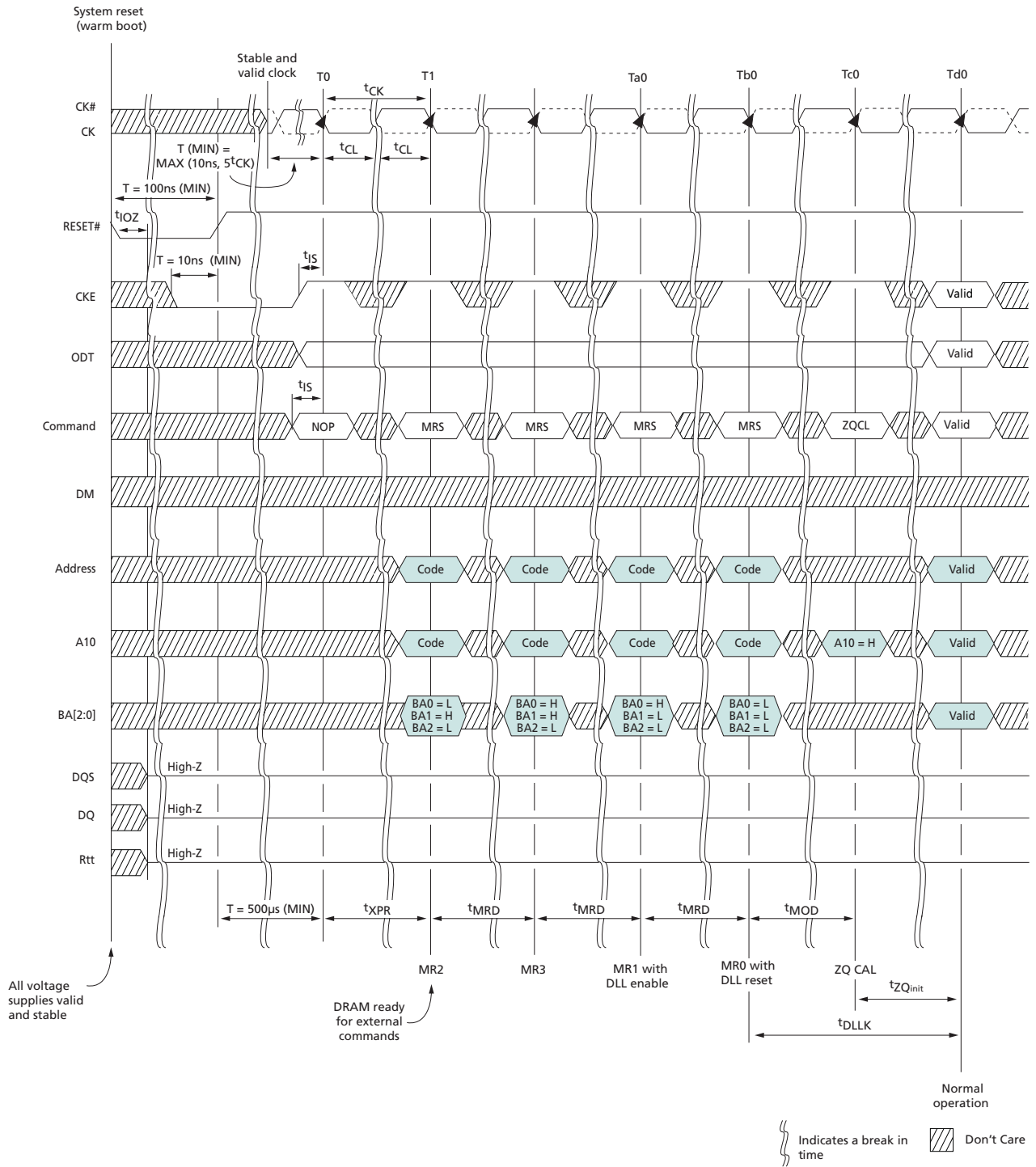
RESET#

The RESET# pin adds stability to the DDR3 memory device. Holding the RESET# pin LOW during power-up ensures that the output pins remain High-Z and that ODT is disabled, and it also resets all internal state machines so that there are no erroneous start-up states. Holding the RESET# pin LOW also internally initializes parts of the DRAM circuitry. With previous generations of DRAM, initialization had to be performed by issuing explicit commands, such as PRECHARGE and AUTO REFRESH.

RESET# is not only useful during initialization of the DDR3 device, but it is also useful during warm boots. It is an asynchronous pin that triggers any time it drops LOW, and there are no restrictions on when it can go LOW. After RESET# goes LOW, all output pins are disabled (High-Z), ODT turns off, and the internal refresh counters and all other relevant circuitry within the DRAM are reset. It must also be assumed that the data stored in the DRAM and the mode register values are unknown after RESET# is brought LOW.

After the DDR3 device is reset, it must be brought up in the predefined manner shown in Figure 3 on page 6. The reset sequence is effectively the same as the initialization sequence the device uses during power-up. The only difference between the reset sequence and the initialization sequence is that the power supplies are already stable in the reset sequence, so RESET# only has to be held LOW for 100ns instead of 200 μ s.

Figure 3: RESET Routine



Mode Registers

Loading the configurable operating parameters into the DDR3 device is performed similarly to the way that configurable operating parameters are loaded in previous generations of DRAM. The DDR3 nomenclature for mode register sets is different than DDR2; for example, DDR2 devices name all mode registers that are beyond the base register as extended registers, and DDR3 devices do not. Regardless of the name differences, many of the modes operate the same way. For more information about available modes, refer to the DDR3 data sheets available on Micron's Web site.

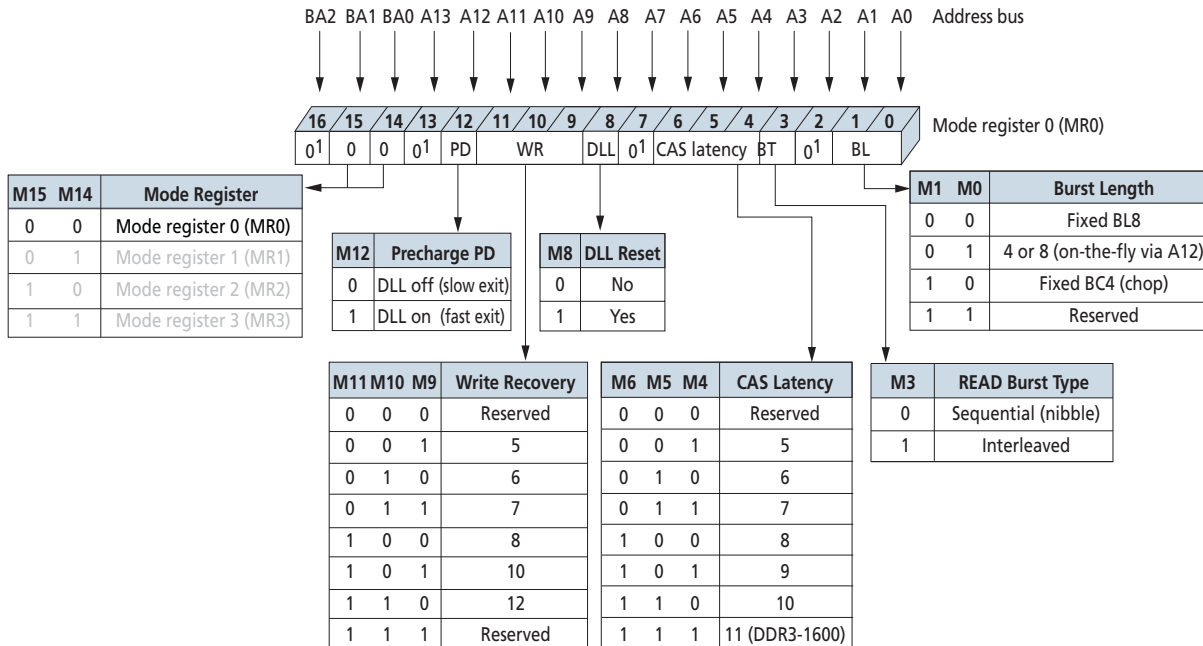
JEDEC defines the sequence in which the mode registers are loaded during the initialization routine (MR2 followed by MR3, MR1, and MR0). Micron tests DDR3 devices using the routine defined by JEDEC and recommends that users follow the same methodology. The mode registers in DDR3 that require special consideration during initialization are discussed in the following sections.

Mode Register 0 (MR0)

The DDR3 base register, mode register 0 (MR0), has effectively the same type of functions as DDR2. These modes include burst length (BL), READ burst type, CAS latency, DLL reset, write recovery (WR), and precharge power-down (PD).

It is important to note that when initializing the DRAM, the DLL must be enabled with MR1 prior to performing the DLL reset in MR0. When the DLL reset bit is enabled, CKE must be HIGH, and the input clock must be held stable for 512 (‘DLLK) clock cycles before a READ command can be issued.

Figure 4: MR0 Definition



Notes: 1. MR0[16, 13, 7, 2] are reserved for future use and must be programmed to 0.

Mode Register 1 (MR1)

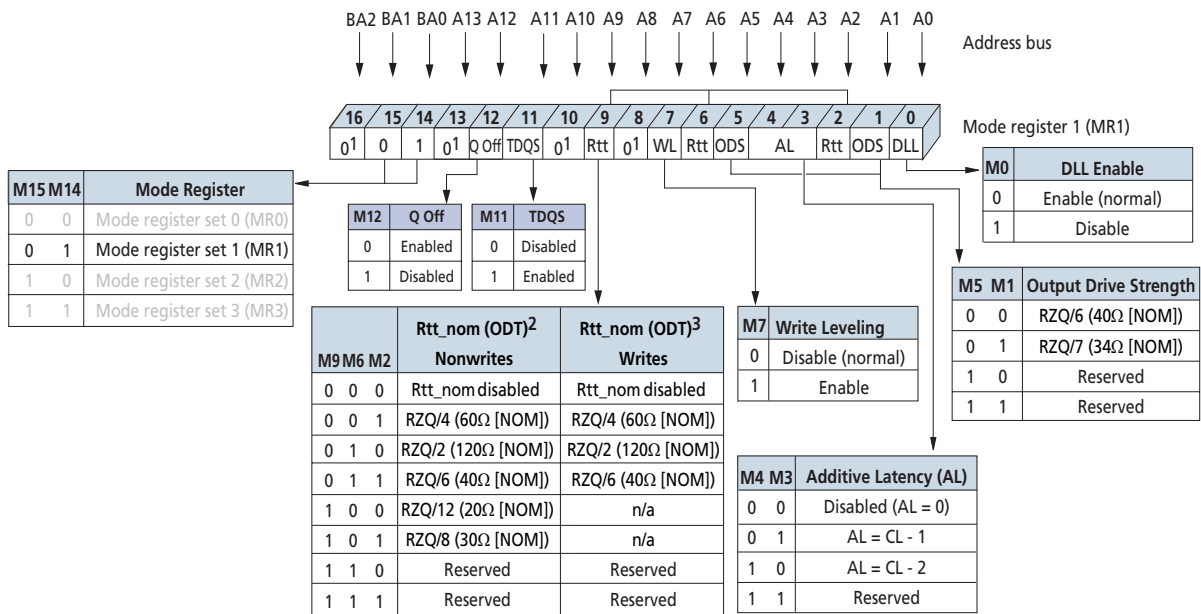
The functions available in mode register 1 (MR1) include DLL enable/disable, output drive strength (ODS), CAS additive latency (AL), write leveling (WL), Rtt_nom value (ODT), TDQS, and Q off (output disable).

To obtain the tight tolerances of the output drive impedance and Rtt_nom values that are selected in MR1, it is necessary to perform the ZQ CALIBRATION LONG (ZQCL) command during the initialization routine. After ZQCL is issued, the t_{ZQinit} timing parameter must be met. During this time, only NOP and DES commands may be issued to the DDR3 device. However, the DLL locking time, also 512 clocks, may be performed in parallel with the ZQ calibration.

For improved signal integrity, DDR3 modules have incorporated a fly-by topology for the address, command, and clock signals. With this new topology, an inherent skew between the DQS and CK must be overcome. Write leveling, a feature in MR1, uses feedback to overcome skew during the initialization routine. Because the write-leveling mode register interacts with many of the other mode registers, it is intended for use after all the other programmable features in mode registers 0–3 are set, and the DLL is fully reset and locked. For more information about how to use write leveling, refer to the DDR3 data sheets available on Micron's Web site.

After the DQS and CK signals for the DDR3 device are aligned, certain steps, which are explained in the DDR3 data sheets, must be performed prior to normal operation. Other than reloading MR1 to turn off write leveling, no other mode registers need to be reloaded prior to normal operation.

Figure 5: MR1 Definition

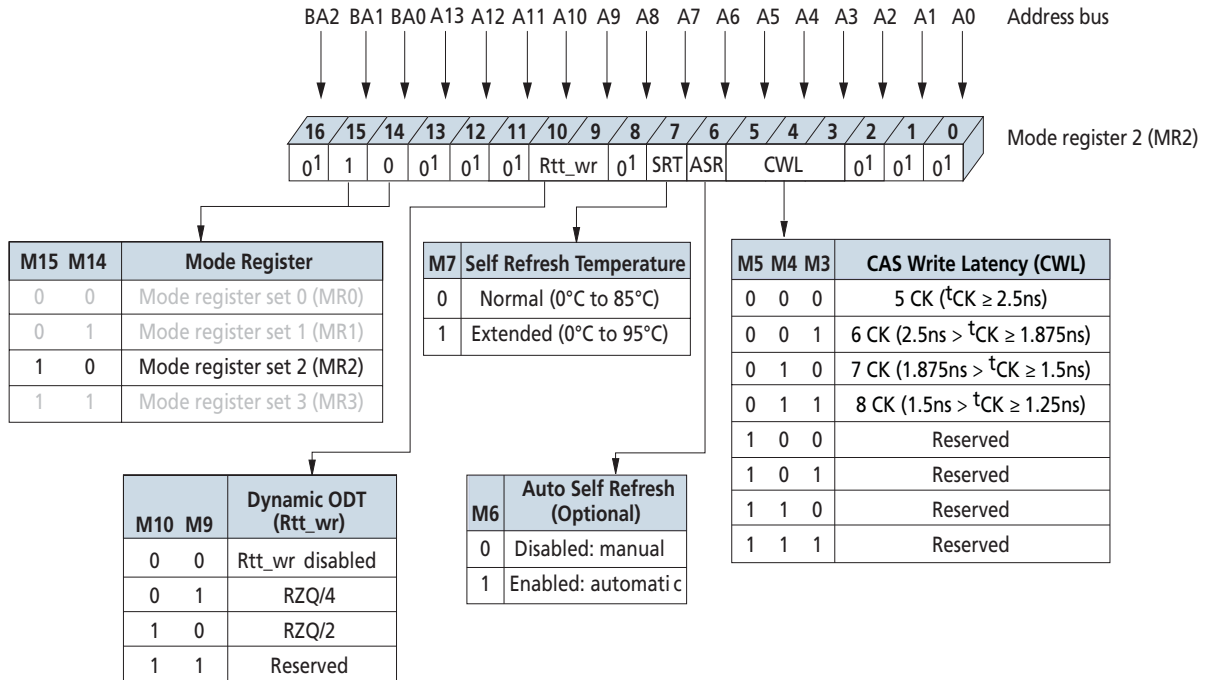


- Notes:
1. MR1[16, 13, 10, 8] are reserved for future use and must be programmed to 0.
 2. During write leveling, if MR1[7] and MR1[12] are 1, then all Rtt_nom values are available for use.
 3. During write leveling, if MR1[7] is a 1 but MR1[12] is a 0, then only Rtt_nom write values are available for use.

Mode Register 2 (MR2)

The functions in mode register 2 (MR2) include CAS write latency (WL), auto self refresh (ASR), self refresh temperature (SRT), and dynamic ODT. Although most of these modes are new with DDR3, none of them require any actions during the initialization routine other than issuance of the standard MRS command with the address bits set at the appropriate levels.

Figure 6: MR2 Definition

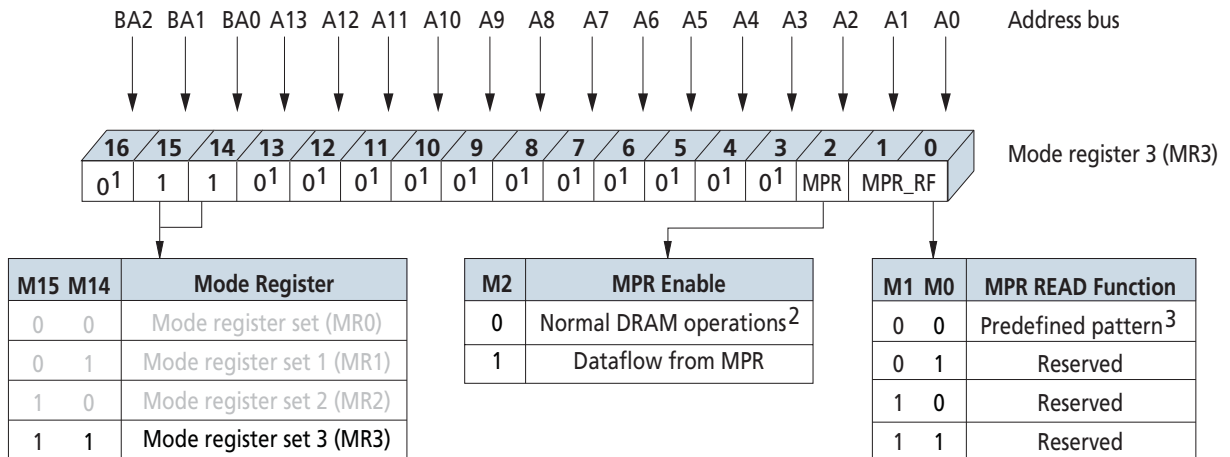


Notes: 1. MR[16, 13:11, 8, and 2:0] are reserved for future use and must be programmed to 0.

Mode Register 3 (MR3)

Currently the only defined function available in mode register 3 (MR3) is the MULTIPURPOSE REGISTER (MPR), which is used to output predefined system timing calibration bit sequences. For more information about the operation of the MPR, refer to the DDR3 data sheets available on Micron's Web site.

Figure 7: MR3 Definition



- Notes:
1. MR3[16 and 13:3] are reserved for future use and must be programmed to 0.
 2. When MPR control is set for normal DRAM operation, MR3[1, 0] will be ignored.
 3. Intended to be used for READ synchronization.

Conclusion

Knowing the selectable modes that require special attention during initialization and then implementing the correct sequence of steps to power up and initialize a DDR3 device will ensure that the device operates properly and is in a known state before normal operation.

For more detail on the use of specific modes available in DDR3, refer to the data sheets and technical notes available on Micron's Web site.



Revision History

Rev. A	10/08
• Initial release	